<table>
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<tr>
<th>Time</th>
<th>Monday</th>
<th>Tuesday</th>
<th>Wednesday</th>
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<tr>
<td>08:00</td>
<td>Registration &amp;</td>
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<td>Breakfast</td>
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<tr>
<td>09:00</td>
<td>Welcome</td>
<td>Keynote 2: Luigi Capodieci, Ph.D., GLOBALFOUNDRIES</td>
<td>Keynote 3: Prof. Erik Brunswald, Univ. of Utah</td>
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<td>A roadmap for DFM and Physical Design</td>
<td>High Performance Ray Tracing: Implications</td>
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<td>at the limits of IC scaling</td>
<td>for System Architectures</td>
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<td>10:15</td>
<td>Coffee break</td>
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<tr>
<td>10:45</td>
<td>Session M1A (3 papers)</td>
<td>T1A: Special Session Memristive Computing</td>
<td>W1A: Special Session</td>
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<td></td>
<td>Electronics for Bio-systems</td>
<td>(3 papers) Networks on Chip</td>
<td>Open Source Tools and</td>
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<td>Methodologies for Research</td>
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<td>12:15</td>
<td>LUNCH</td>
<td>LUNCH</td>
<td>Session W1B (4 papers)</td>
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<td>13:45</td>
<td>Session M2A (3 papers)</td>
<td>Session T9A (3 papers) Verification and Fault</td>
<td>Session W2A (3 papers)</td>
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<td>Transistor Level Digital</td>
<td>Tolerance</td>
<td>FPGA Design and Optimization</td>
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<td>15:15</td>
<td>POSTER Session 1</td>
<td>Session T9B (3 papers) Multi-core and embedded</td>
<td>Session W2B (3 papers) Power and temperature</td>
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<td>Coffee Break</td>
<td>SoC</td>
<td>management</td>
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<tr>
<td>16:15</td>
<td>Session M3A (3 papers)</td>
<td>PhD Forum</td>
<td>Concluding Remarks &amp; Best Paper Award</td>
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<td></td>
<td>Analog &amp; Mixed Signal Design</td>
<td>(3 papers) Digital Circuits and Systems 1</td>
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## MONDAY

### Registration & Breakfast  
08:00-09:00

### Welcome  
09:00-09:15

### Keynote 1: Prof. Yusuf Leblebici, EPFL  
09:15-10:15  
Design and Testing Strategies for Modular 3D-Multiprocessor

### Coffee break  
10:15-10:45

### Session M1A: Electronics for Bio-systems  
10:45-12:15

- Le Zheng, Sangho Shin and Sung-Mo Kang. Design of a Neural Stimulator System with Closed-Loop Charge Cancellation
- Kenneth O’Neal, Daniel Grissom and Philip Brisk. Force-directed List Scheduling for Digital Microfluidic Biochips
- Surya Sharma and Trond Ytterdal. Low Noise Front-end Amplifier Design for Medical Ultrasound Imaging Applications

### Session M1B: Networks on Chip  
10:45-12:15

- Mingyang Zhu, Jinho Lee and Kiyoungh Choi. An adaptive routing algorithm for 3D mesh NoC with limited vertical bandwidth
- Giulia Beanato, Igor Loi, Giovanni De Micheli, Yusuf Leblebici and Luca Benini. 3D-LIN: A Configurable Low-Latency Interconnect for Multi-Core Clusters with 3D Stacked L1 Memory

### Lunch  
12:15-13:45

### Session M2A: Transistor Level Digital Circuits  
13:45-15:15

- Ruixing Li, Na Bai, Junning Chen, Weiqi Wu, Qunling Yu and Mingqiang Qiu. Design of a new current-mode sense amplifier combined with leakage current compensation for high-performance SRAM
- Stefano Pietri, Alfredo Olmos, Chris Dao and Juxiang Ren. Safety Oriented automotive MCU power management
- Farhad Parsan and Scott Smith. CMOS Implementation of Static Threshold Gates with Hysteresis: A New Approach

### Embedded Tutorial  
13:45-15:15

Silicon Photonics Circuits and Architectures for Many-Core Systems
POSTER Session 1 & Coffee break

- Bahareh Beheshti, Mohsen Jalali and Mehdi Lotfi Navaii. A New Low-Power Noncoherent BPSK Demodulator for Biomedical Applications
- Andy Motten and Luc Claesen. Trinocular Disparity Processor using a Hierarchic Classification Structure
- Christina Gimmler-Dumont, Christian Brehm and Norbert Wehn. Reliability Study on System Memories of an Iterative MIMO-BICM System
- Hamed Sajjadi-Kia and Cristinel Ababei. A New Reliability Evaluation Methodology and its Application to Network-on-Chip Routers
- Victor Silva, Flavio Wagner and Cantidio Fontes. The Impact of Synchronization in Message Passing While Scaling Multi-core MPSoC Systems
- Chirag Ravishankar, Andrew Kennings and Jason Anderson. FPGA Power Reduction by Guarded Evaluation Considering Physical Information
- Jaspal Singh Shah, David Nairn and Manoj Sachdev. A Soft Error Robust 32kb SRAM Macro Featuring Access Transistor-Less 8T Cell in 65-nm

Session M3A: Analog & Mixed Signal Design

- Ali Mesgarani, Hao Yu and Suat Ay. A 6-bit 1.5GS/s Pipelined Binary Search ADC with Simplified Clocking Scheme
- Sohail Asghar, Rocío Del Río and Jose M. de La Rosa. A 0.2-to-2MHz BW, 50-to-86dB SNDR, 16-to-22mW Flexible 4th-Order Sigma-Delta Modulator with DC-to-44MHz Tunable Center Frequency in 1.2-V 90-nm CMOS

Session M3B: Digital Circuits and Systems I

- Haven Skinner, Xuchu Hu and Matthew Guthaus. Harmonic Resonant Clocking
- Andreas Minwegen, Dominik Auras and Gerd Ascheid. A Multimode Decision-Directed Channel Estimation ASIC for MIMO-OFDM
- Christian Benkeser, Christoph Roth and Qiuting Huang. Turbo Decoder Design for High Code Rates
TUESDAY

Registration & Breakfast 08:00-09:00

Keynote 2: Luigi Capodieci, Ph.D., GLOBAL FOUNDRIES 09:00-10:00
A roadmap for DFM and Physical Design at the limits of IC scaling

Coffee break 10:00-10:30

Special Session T1A: Memristive Computing 10:30-12:30
- Fernando Corinto, Alon Ascoli and Marco Gilli. A novel elementary memristive system
- Dmitri Strukov and Advait Madhavan. Mapping Image and Network Processing Tasks onto High-Throughput CMOL FPGA Circuits
- Dmitri Strukov, Ligang Gao and Fabien Alibart. Analog-Input Analog-Weight Dot Product Operation with Ag/a-Si/Pt Memristive Devices
- Pierre-Emmanuel Gaillardon, Davide Sacchetto, Shashikanth Bobba and Yusuf Leblebici. GMS: Generic Memristive Structure Concept for 3-D FPGAs
- Ravi Patel and Eby Friedman. Arithmetic Encoding for Memristive Multi-Bit Storage

Session T1B: Digital Circuits and Systems II 10:30-12:30
- Qiuling Zhu, Larry Pileggi and Franz Franchetti. Cost-Effective Smart Memory Implementation for Parallel Backprojection in Computed Tomography
- Michael Muehlberghuber, Christoph Keller, Norbert Felber and Christian Pendl. 100 Gbit/sAuthenticated Encryption Based on Quantum Key Distribution

Lunch 12:30-14:00

Session T2A: Verification and Fault Tolerance 14:00-15:30
- Davide Sabena, Matteo Sonza Reorda and Luca Sterpone. A new method for the automatic generation of optimized Software-Based Self-Test programs for VLIW processors.
- Sebastian Steinhorst and Lars Hedrich. Equivalence Checking of Nonlinear Analog Circuits for Hierarchical AMS System Verification
- Shilpa Pendyala and Srinivas Katkooi. Interval Arithmetic Based Input Vector Control for RTL Subthreshold Leakage Minimization

Session T2B: Multi-core and embedded SoC 14:00-15:30
- Radu David, Paul Bogdan and Radu Marculescu. Dynamic Power Management for Multicores: Case Study Using the Intel SCC
- Zhibin Xiao and Bevan Baas. A Hexagonal Shaped Processor and Interconnect Topology for Tightly-tiled Many-Core Architecture
Jeremy Constantin, Ahmed Dogan, Oskar Andersson, Pascal Meinerzhagen, Joachim Neves Rodrigues, David Atienza and Andreas Burg. An Ultra-Low-Power Application-Specific Processor for Compressed Sensing

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<th>Event</th>
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<tr>
<td>PhD Forum</td>
<td>15:30-16:30</td>
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<td>Panel Session</td>
<td>16:30-18:00</td>
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<tr>
<td>Conference Banquet</td>
<td>19:45-23:00</td>
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**WEDNESDAY**

**Registration & Breakfast** 08:00-09:00

**Keynote 3: Prof. Erik Brunvand, Univ. of Utah** 09:00-10:00
High Performance Ray Tracing: Implications for System Architectures

**Coffee break** 10:00-10:30

**Special Session W1A: Open Source Tools and Methodologies for Research** 10:30-12:30
- Niket Choudhary, Brandon Dwiel and Eric Rotenberg. A Physical Design Study of FabScalar-generated Superscalar Cores
- Anton Tšepurov, Günter Bartsch, Rainer Dorsch, Maksim Jenihihin, Jaan Raik and Valentin Tihomirov. A Scalable Model Based RTL Framework zamiaCAD for Static Analysis
- Gregory Faust, Runjie Zhang, Kevin Skadron, Mircea Stan and Brett Meyer. ArchFP: Rapid Prototyping of pre-RTL Floorplans

**Session W1B: Design for reliability** 10:30-12:30
- Hamid Mahmoodi. Reliability Enhancement of Power Gating Transistor under Time Dependant Dielectric Breakdown
- Muhammad Tauseef Rab, Asad A. Bawa and Nur A. Touba. Using Asymmetric Layer Repair Capability to Reduce the Cost of Yield Enhancement in 3D Stacked Memories
- Tasreen Charania. Suppression of On-Chip Power Supply Noise Generated by a 64-Bit Static Logic ALU Block
- Seokjoong Kim and Matthew Guthaus. Dynamic Voltage Scaling for SEU-Tolerance in Low-Power Memories

**Lunch** 12:30-14:00

**Session W2A: FPGA Design and Optimization** 14:00-15:30
- Krishna Chaitanya Nunna, Farhad Mehdipour and Kauuki Murakami. Methodology for Early Estimation of Hierarchical Routing Resources in 3D FPGAs
- Yuki Nishitani, Kazuki Inoue, Motoki Amagasaki, Masahiro Iida, Morihiro Kuga and Toshinori Sueyoshi. Evaluation of Fault Tolerant Technique Based on Homogeneous FPGA Architecture

**Session W2B: Power and temperature management** 14:00-15:30
- Bin Wu and Peng Li. Loadaware Stochastic Feedback Control for DVFS with Tight Performance Guarantee
- Haroon Mahmood, Massimo Poncino, Mirko Loghi and Enrico Macii. Aging-Aware Caches with Graceful Degradation of Performance
- Jie Meng, Fulya Kaplan, Ting-Yu Hsieh and Ayse Coskun. Topology-Aware Reliability Optimization for Multiprocessor Systems
**POSTER 2: WEDNESDAY**

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<tr>
<th>Time</th>
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<tr>
<td>15:30-16:30</td>
<td>Successive Interference Cancellation for 3G Downlink: Algorithm and VLSI Architecture</td>
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<tr>
<td>15:30-16:30</td>
<td>A High-throughput and Low-Latency Interconnection Network for Multi-Core Clusters with 3-D Stacked L2 Tightly-Coupled Data Memory</td>
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<td>15:30-16:30</td>
<td>Low Cost Adjacent Double Error Correcting Code with Complete Elimination of Miscorrection Within a Dispersion Window for Multiple Bit Upset Tolerant Memory</td>
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<td>15:30-16:30</td>
<td>Impact of Technology Scaling on Performance of Domino Logic in Nano-Scale CMOS</td>
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<td>15:30-16:30</td>
<td>Application-guided Reliability-enhanced Registerfile Architecture for Embedded Processors</td>
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<td>15:30-16:30</td>
<td>A Complete Over-Current/Short-Circuit Protection System for Low-Drop Out Regulators</td>
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<td>Low power SoCs with Resonant Dynamic Logic using Inductors for Energy Recovery</td>
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<td>15:30-16:30</td>
<td>Efficient Adaptive Switch Design for Charge pumps in Micro-scale Energy Harvesting</td>
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**Concluding remarks & Best paper awards**  
16:30-17:00