VLSI-SoC 2012 Technical Program

	Monday	Tuesday	Wednesday	
08:00	Registration & Breakfast	Registration & Breakfast	Registration & Breakfast	08:00
09:00	Welcome	Keynote 2: Luigi Capodieci, Ph.D., GLOBALFOUNDRIES A roadmap for DFM and Physical Design at the limits of IC scaling **Room: Surf view**	Keynote 3: Prof. Erik Brunvand, Univ. of Utah High Performance Ray Tracing: Implications for System Architectures **Room: Surf view**	09:00
09:15	Keynote 1: Prof. Yusuf Leblebici, EPFL Design and Testing Strategies for Modular 3D-Multiprocessor **Room: Surf view**			
10:15	Coffee break	Coffee break	Coffee break	10:00
10:45	Session M1A Electronics for Bio-systems Chair: Paul Hurst **Room: Surf view** Session M1B Networks on Chip Chair: Paul Franzon **Room: Beach view**	T1A: Special Session Memristive Computing Chair: Steve Kang **Room: Surf view** Session T1B Digital Circuits and Systems II Chair: Luc Claessen **Room: Beach view**	W1A: Special Session Open Source Tools and Methodologies for Research Chair: Jose Renau **Room: Surf view** Session W1B Design for reliability Chair: Mirko Loghi **Room: Beach view**	10:30
12:15	LUNCH	LUNCH	LUNCH	12:30
13:45	Embedded Tutorial Silicon Photonics Circuits and Architectures for Many-Core Systems **Room: Surf view** Session M2A Transistor Level Digital Chair: Fernanda Kastensmidt **Room: Beach view**	Session T2A Verification and Fault Tolerance Chair: Anupam Chattopadhyay **Room: Surf view** Session T2B Multi-core and embedded SoC Chair: Philip Brisk **Room: Beach view**	Session W2A FPGA Design and Optimization Chair: Pierre-Emmanuel Gaillardo **Room: Surf view** Session W2B Power and temperature management Chair: Hamid Mahmoodi **Room: Beach view**	14:00
15:15	POSTER Session 1 & Coffee break Chair: Christian Benkeser	PhD Forum & Coffee Break	POSTER Session 2 & Coffee Break Chair: Flavio Wagner	15:30
16:15	Session M3A Analog & Mixed Signal Design Chair: Ligang Gao **Room: Surf view** Session M3B Digital Circuits and Systems I Chair: Sergio Bampi **Room: Beach view**	PANEL Organizer: Prof. Sergio Bampi Analog VLSI Design at the End of CMOS Scaling: What is ahead? **Room: Surf view**	Concluding Remarks & Best Paper Award **Room: Surf view**	16:30
17:45				

MONDAY

Registration & Breakfast **08:00-09:00**

Welcome **09:00-09:15**

Keynote 1: Prof. Yusuf Leblebici, EPFL **09:15-10:15**
Design and Testing Strategies for Modular 3D-Multiprocessor

Coffee break **10:15-10:45**

Session M1A: Electronics for Bio-systems **10:45-12:15**
Chair: Paul Hurst

- Le Zheng, Sangho Shin and Sung-Mo Kang. Design of a Neural Stimulator System with Closed-Loop Charge Cancellation
- Kenneth O'Neal, Daniel Grissom and Philip Brisk. Force-directed List Scheduling for Digital Microfluidic Biochips
- Surya Sharma and Trond Ytterdal. Low Noise Front-end Amplifier Design for Medical Ultrasound Imaging Applications

Session M1B: Networks on Chip **10:45-12:15**
Chair: Paul Franzon

- Mingyang Zhu, Jinho Lee and Kiyoung Choi. An adaptive routing algorithm for 3D mesh NoC with limited vertical bandwidth
- Anelise Kologeski, Caroline Concatto, Fernanda Kastensmidt and Luigi Carro. ATARDS: An Adaptive Fault-Tolerant Strategy to Cope with Massive Defects in Network-on-Chip Interconnections
- Giulia Beanato, Igor Loi, Giovanni De Micheli, Yusuf Leblebici and Luca Benini. 3D-LIN: A Configurable Low-Latency Interconnect for Multi-Core Clusters with 3D Stacked L1 Memory

Lunch **12:15-13:45**

Session M2A: Transistor Level Digital Circuits **13:45-15:15**
Chair: Fernanda Kastensmidt

- Stefano Pietri, Alfredo Olmos, Chris Dao and Juxiang Ren. Safety Oriented automotive MCU power management
- Farhad Parsan and Scott Smith. CMOS Implementation of Static Threshold Gates with Hysteresis: A New Approach

Embedded Tutorial **13:45-15:15**
Silicon Photonics Circuits and Architectures for Many-Core Systems

POSTER Session 1 & Coffee break **15:15-16:15**
Chair: Christian Benkeser

- Andy Motten and Luc Claesen. Trinocular Disparity Processor using a Hierarchic Classification Structure
- Anupam Chattopadhyay and Goutam Paul. Exploring Security-Performance Trade-offs during Hardware Accelerator Design of Stream Cipher RC4
- Christina Gimmler-Dumont, Christian Brehm and Norbert Wehn. Reliability Study on System Memories of an Iterative MIMO-BICM System
- Hamed Sajjadi-Kia and Cristinel Ababei. A New Reliability Evaluation Methodology and its Application to Network-on-Chip Routers
- Jongpil Jung, Kyungsu Kang and Chong-Min Kyung. Cost-effective TSV Redundancy Configuration
- Victor Silva, Flavio Wagner and Cantidio Fontes. The Impact of Synchronization in Message Passing While Scaling Multi-core MPSoC Systems
- Chirag Ravishankar, Andrew Kennings and Jason Anderson. FPGA Power Reduction by Guarded Evaluation Considering Physical Information
- Jaspal Singh Shah, David Nairn and Manoj Sachdev. A Soft Error Robust 32kb SRAM Macro Featuring Access Transistor-Less 8T Cell in 65-nm
- Ilias Pappas, Stylianos Siskos, Vasileios Kalenteridis and Spyridon Vlassis. A Complete Over-Current/Short-Circuit Protection System for Low-Drop Out Regulators

Session M3A: Analog & Mixed Signal Design **16:15-17:45**
Chair: Ligang Gao

- Sohail Asghar, Rocío Del Río and Jose M. de La Rosa. A 0.2-to-2MHz BW, 50-to-86dB SNDR, 16-to-22mW Flexible 4th-Order Sigma-Delta Modulator with DC-to-44MHz Tunable Center Frequency in 1.2-V 90-nm CMOS
- ***** Neil Di Spigna, Daniel Schinke, Srikant Jayanti, Veena Misra and Paul Franzon. A Novel Double Floating-Gate Unified Memory Device

Session M3B: Digital Circuits and Systems I **16:15-17:45**
Chair: Sergio Bampi

- Haven Skinner, Xuchu Hu and Matthew Guthaus. Harmonic Resonant Clocking
- Andreas Minwegen, Dominik Auras and Gerd Ascheid. A Multimode Decision-Directed Channel Estimation ASIC for MIMO-OFDM
- Christian Benkeser, Christoph Roth and Qiuting Huang. Turbo Decoder Design for High Code Rates

TUESDAY

Registration & Breakfast **08:00-09:00**

Keynote 2: Luigi Capodieci, Ph.D., GLOBAL FOUNDRIES **09:00-10:00**
A roadmap for DFM and Physical Design at the limits of IC scaling

Coffee break **10:00-10:30**

Special Session T1A: Memristive Computing **10:30-12:30**
Chair: Steve Kang

- Fernando Corinto, Alon Ascoli and Marco Gilli. A novel elementary memristive system
- Dmitri Strukov and Advait Madhavan. Mapping Image and Network Processing Tasks onto High-Throughput CMOL FPGA Circuits
- Dmitri Strukov, Ligang Gao and Fabien Alibart. Analog-Input Analog-Weight Dot Product Operation with Ag/a-Si/Pt Memristive Devices
- Pierre-Emmanuel Gaillardon, Davide Sacchetto, Shashikanth Bobba and Yusuf Leblebici. GMS: Generic Memristive Structure Concept for 3-D FPGAs
- Ravi Patel and Eby Friedman. Arithmetic Encoding for Memristive Multi-Bit Storage

Session T1B: Digital Circuits and Systems II **10:30-12:30**
Chair: Luc Claessen

- Pierre Greisen, Richard Emler, Michael Schaffner, Simon Heinzle and Frank Gürkaynak. A General-Transformation EWA View Rendering Engine for 1080p Video in 130 nm CMOS
- Qiuling Zhu, Larry Pileggi and Franz Franchetti. Cost-Effective Smart Memory Implementation for Parallel Backprojection in Computed Tomography
- Cristiano Thiele, Bruno B. Vizzotto, Andre Martins, Vagner Rosa and Sergio Bampi. A Low-Cost and High Efficiency Entropy Encoder Architecture for H.264/AVC
- Michael Muehlberghuber, Christoph Keller, Norbert Felber and Christian Pendl. 100 Gbit/s Authenticated Encryption Based on Quantum Key Distribution

Lunch **12:30-14:00**

Session T2A: Verification and Fault Tolerance **14:00-15:30**
Chair: Anupam Chattopadhyay

- ***** Davide Sabena, Matteo Sonza Reorda and Luca Sterpone. A new method for the automatic generation of optimized Software-Based Self-Test programs for VLIW processors.
- Sebastian Steinhorst and Lars Hedrich. Equivalence Checking of Nonlinear Analog Circuits for Hierarchical AMS System Verification
- Shilpa Pendyala and Srinivas Katkoori. Interval Arithmetic Based Input Vector Control for RTL Subthreshold Leakage Minimization

Session T2B: Multi-core and embedded SoC 14:00-15:30
Chair: Philip Brisk

- Radu David, Paul Bogdan and Radu Marculescu. Dynamic Power Management for Multicores: Case Study Using the Intel SCC
- Zhibin Xiao and Bevan Baas. A Hexagonal Shaped Processor and Interconnect Topology for Tightly-tiled Many-Core Architecture
- ***** Jeremy Constantin, Ahmed Dogan, Oskar Andersson, Pascal Meinerzhagen, Joachim Neves Rodrigues, David Atienza and Andreas Burg. An Ultra-Low-Power Application-Specific Processor for Compressed Sensing

PhD Forum **15:30-16:30**

Panel Session **16:30-18:00**

Conference Banquet **19:45-23:00**

WEDNESDAY

Registration & Breakfast **08:00-09:00**

Keynote 3: Prof. Erik Brunvand, Univ. of Utah **09:00-10:00**
High Performance Ray Tracing: Implications for System Architectures

Coffee break **10:00-10:30**

Special Session W1A: Open Source Tools and Methodologies for Research **10:30-12:30**
Chair: Jose Renau

- Niket Choudhary, Brandon Dwiel and Eric Rotenberg. A Physical Design Study of FabScalar-generated Superscalar Cores
- Anton Tšepurov, Günter Bartsch, Rainer Dorsch, Maksim Jenihhin, Jaan Raik and Valentin Tihhomirov. A Scalable Model Based RTL Framework zamiaCAD for Static Analysis
- Daniel Grissom, Kenneth O'Neal, Benjamin Preciado, Hiral Patel, Robert Doherty, Nick Liao and Philip Brisk. A Digital Microfluidic Biochip Synthesis Framework
- Gregory Faust, Runjie Zhang, Kevin Skadron, Mircea Stan and Brett Meyer. ArchFP: Rapid Prototyping of pre-RTL Floorplans

Session W1B: Design for reliability **10:30-12:30**
Chair: Mirko Loghi

- Hamid Mahmoodi. Reliability Enhancement of Power Gating Transistor under Time Dependant Dielectric Breakdown
- Muhammad Tauseef Rab, Asad A. Bawa and Nur A. Touba. Using Asymmetric Layer Repair Capability to Reduce the Cost of Yield Enhancement in 3D Stacked Memories
- Tasreen Charania. Suppression of On-Chip Power Supply Noise Generated by a 64-Bit Static Logic ALU Block
- ***** Seokjoong Kim and Matthew Guthaus. Dynamic Voltage Scaling for SEU-Tolerance in Low-Power Memories

Lunch **12:30-14:00**

Session W2A: FPGA Design and Optimization **14:00-15:30**
Chair: Pierre-Emmanuel Gaillardo

- Krishna Chaitanya Nunna, Farhad Mehdipour and Kazuaki Murakami. Methodology for Early Estimation of Hierarchical Routing Resources in 3D FPGAs
- Rajsaktish Sankaranarayanan and Matthew Guthaus. A Single-VDD Ultra-Low Energy Sub-threshold FPGA
- Yuki Nishitani, Kazuki Inoue, Motoki Amagasaki, Masahiro Iida, Morihiro Kuga and Toshinori Sueyoshi. Evaluation of Fault Tolerant Technique Based on Homogeneous FPGA Architecture

Session W2B: Power and temperature management 14:00-15:30
Chair: Hamid Mahmoodi

- Bin Wu and Peng Li. Loadaware Stochastic Feedback Control for DVFS with Tight Performance Guarantee
- Haroon Mahmood, Massimo Poncino, Mirko Loghi and Enrico Macii. Aging-Aware Caches with Graceful Degradation of Performance
- Jie Meng, Fulya Kaplan, Ming-Yu Hsieh and Ayse Coskun. Topology-Aware Reliability Optimization for Multiprocessor Systems

POSTER 2: WEDNESDAY 15:30-16:30
Chair: Flavio Wagner

- Sandro Belfanti, Christian Benkeser, Karim Badawi, Qiuting Huang and Andreas Burg. Successive Interference Cancellation for 3G Downlink: Algorithm and VLSI Architecture
- Kyungsu Kang, Luca Benini and Giovanni De Micheli. A High-throughput and Low-Latency Interconnection Network for Multi-Core Clusters with 3-D Stacked L2 Tightly-Coupled Data Memory
- Avijit Dutta. Low Cost Adjacent Double Error Correcting Code with Complete Elimination of Miscorrection Within a Dispersion Window for Multiple Bit Upset Tolerant Memory
- Takeshi Matsumoto, Shohei Ono and Masahiro Fujita. An Efficient Method to Localize and Correct Bugs in High-Level Designs Using Counterexamples and Potential Dependence
- Abhishek Guar and Hamid Mahmoodi. ¬¬¬Impact of Technology Scaling on Performance of Domino Logic in Nano-Scale CMOS
- Hamed Tabkhi and Gunar Schirner. ARRA: Application-guided Reliability-enhanced Registerfile Architecture for Embedded Processors
- Ignatius Bezzam, Shoba Krishnan and Chakravarthy Mathiazhagan. Low power SoCs with Resonant Dynamic Logic using Inductors for Energy Recovery
- Hafeez Kt, Ashudeb Dutta and Shiv Govind Singh. Efficient Adaptive Switch Design for Charge pumps in Micro-scale Energy Harvesting

Concluding remarks & Best paper awards 16:30-17:00